AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original) Apparatus for processing data under control of data processing instructions specifying data processing operations, said apparatus comprising:

a first execution mechanism (130) operable to execute a first set of data processing instructions;

a second execution mechanism operable to execute a second set of data processing instructions, said first set of data processing instructions overlapping with said second set of data processing instructions such that one or more data processing instructions are executable by either said first execution mechanism or said second execution mechanism; and

an execution mechanism selector (140) operable to pseudo randomly selected either said first execution mechanism or said second execution mechanism to execute one or more data processing instructions that are executable by either said first execution mechanism or said second execution mechanism; wherein said execution mechanism selector is controlled by a pseudo random execution mechanism selecting signal (j2 ran) generated by a pseudo random signal generator.

2. (original) Apparatus as claimed in claim 1, wherein said first execution mechanism and said second execution mechanism have at least one different execution

characteristic for at least one of said data processing instructions that are executable by either said first execution mechanism or said second execution mechanism.

3. (original) Apparatus as claimed in claim 2, wherein said at least one different execution characteristic includes one or more of:

time to execute said data processing instruction; and

power consumption when executing said data processing instruction.

4. (currently amended) Apparatus as claimed in ~~any one of claims 2 and 3~~ claim 2, wherein at least one execution characteristic of at least one data processing instruction executed by one of said first execution mechanism or said second execution mechanism varies in dependence upon whether a preceding data processing instruction was executed with either said first execution mechanism or said second execution mechanism.

5. (currently amended) Apparatus as claimed in ~~any one of the preceding claims~~ claim 1, wherein all of said data processing instructions are executable by either said first execution mechanism or said second execution mechanism.

6. (currently amended) Apparatus as claimed in ~~any one of the preceding claims~~ claim 1, wherein said first execution mechanism is operable to execute some of said data processing instructions as native instructions directly controlling data processing

hardware and remaining data processing instructions using emulation software.

7. (currently amended) Apparatus as claimed ~~in any one of the preceding claims~~ claim 1, wherein said second execution mechanism is operable to execute all of said data processing instructions using emulation software.

8. (currently amended) Apparatus as claimed in ~~claims 6 and 7~~ claim 6, wherein said first execution mechanism and said second execution mechanism share at least some emulation software.

9. (currently amended) Apparatus as claimed in ~~any one of the preceding claims~~ claim 1, wherein said data processing instructions are Java bytecode instructions.

10. (original) Apparatus as claimed in claim 9, wherein said first execution mechanism includes native Java bytecode execution hardware and said second execution mechanism uses Java bytecode emulation for all Java bytecodes.

11. (original) Apparatus as claimed in claim 1, comprising a processor core, said pseudo random execution mechanism selecting signal being an input to said processor core.

12. (currently amended) Apparatus as claimed in ~~any one of the preceding claims~~

claim 1, wherein a system configuration parameter is operable to force said execution mechanism selector to select said first execution mechanism for all data processing instructions.

13. (original) Apparatus as claimed in claim 12, wherein said system configuration parameter is stored in a system configuration register.

14. (original) A method of processing data under control of data processing instructions specifying data processing operations, said method comprising the steps of:

executing a first set of data processing instructions with a first execution mechanism;

executing a second set of data processing instructions with a second execution mechanism, said first set of data processing instructions overlapping with said second set of data processing instructions such that one or more data processing instructions are executable by either said first execution mechanism or said second execution mechanism; and

pseudo randomly selecting with an execution mechanism selector either said first execution mechanism or said second execution mechanism to execute one or more data processing instructions that are executable by either said first execution mechanism or said second execution mechanism; wherein said execution mechanism selector is controlled by a pseudo random execution mechanism selecting signal generated by a pseudo random signal generator.

15. (original) A method as claimed in claim 14, wherein said first execution mechanism and said second execution mechanism have at least one different execution characteristic for at least one of said data processing instructions that are executable by either said first execution mechanism or said second execution mechanism.

16. (original) A method as claimed in claim 15, wherein said at least one different execution characteristic includes one or more of:

time to execute said data processing instruction; and

power consumption when executing said data processing instruction.

17. (currently amended) A method as claimed in ~~any one of claims 15 and 16~~ claim 15, wherein at least one execution characteristic of at least one data processing instruction executed by one of said first execution mechanism or said second execution mechanism varies in dependence upon whether a preceding data processing instruction was executed with either said first execution mechanism or said second execution mechanism.

18. (currently amended) A method as claimed in ~~any one of claims 14 to 17~~ claim 14, wherin all of said data processing instructions are executable by either said first execution mechanism or said second execution mechanism.

19. (currently amended) A method as claimed in ~~any one of claims 14 to 18~~ claim 14, wherein said first execution mechanism is operable to execute some of said data processing instructions as native instructions directly controlling data processing hardware and remaining data processing instructions using emulation software.

20. (currently amended) A method as claimed in ~~any one of claims 14 to 19~~ claim 14, wherein said second execution mechanism is operable to execute all of said data processing instructions using emulation software.

21. (currently amended) A method as claimed in ~~claims 19 and 20~~ claim 19, wherein said first execution mechanism and said second execution mechanism share at least some emulation software.

22. (currently amended) A method as claimed in ~~any one of claims 14 to 21~~ claim 14, wherein said data processing instructions are Java bytecode instructions.

23. (original) A method as claimed in claim 22, wherein said first execution mechanism includes native Java bytecode execution hardware and said second execution mechanism uses Java bytecode emulation *for* all Java bytecodes,

24. (original) A method as claimed in claim 14, comprising a processor core, said pseudo random execution mechanism selecting signal being an input to said processor

core.

25. (currently amended) A method as claimed in ~~any one of claims 14 to 24~~ claim 14, wherein a system configuration parameter is operable to force said execution mechanism selector to select said first execution mechanism for all data processing instructions.

26. (original) A method as claimed in claim 25, wherein said system configuration parameter is stored in a system configuration register.